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COMPUTER ARCHITECTURE TECHNIQUES FOR POWER-EFFICIENCY

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Power dissipation issues have catalyzed new topic areas in computer architecture, resulting in a substantial body of work on more power-efficient architectures. Power dissipation coupled with diminishing performance gains, was also the main cause for the switch from single-core to multi-core architectures and a slowdown in frequency increase.

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Network Processor Design, Volume 2: Issues and Practices, Volume 2 (The Morgan Kaufmann Series in Computer Architecture and Over the past ten years, architecture techniques for power efficiency have

shifted from primarily focusing on module-level efficiencies, toward more holistic design styles based on parallelism and heterogeneity.

COMPUTER ARCHITECTURE TECHNIQUES FOR POWER-EFFICIENCY MOBI ...
Computer architecture techniques and power dissipation The cache hierarchy Placement policies I Direct Mapped: lower bits of block @ index cache line Simple logic, many con?ict misses. I Fully Associative: block can be placed in any cache line Compare each cache line’s tag (CAM: Content Addressable Memory) Complex (slow or small) logic, fewer misses.

Computer architecture techniques and power dissipation
Computer Architecture Techniques for Power-Efficiency: Kaxiras, Stefanos: Amazon.com.au: Books

Computer Architecture Techniques for Power-Efficiency ...
ACM Transactions on Architecture and Code Optimization (TACO), 2015. == Book: == NEW! Our new book is out: "Power-Efficient Computer Architectures: Recent Advances" Paperback, Morgan and Claypool Publishers, January 1, 2015 by Magnus Sjalander, Margaret Martonosi, Stefanos Kaxiras. Computer Architecture Techniques for Power-Efficiency

Stefanos Kaxiras - Department of Information Technology ...
A computer system is basically a machine that simplifies complicated tasks. It should maximize performance and reduce costs as well as power consumption.The dif ...

Computer System Architecture - Tutorialspoint
What is Computer Architecture? • “Computer Architecture is the science and art of selecting and interconnecting hardware components to create computers that meet functional, performance and cost goals.” - WWW Computer Architecture Page • An analogy to architecture of buildings… CIS 501 (Martin): Introduction 3

What is Computer Architecture?
Power dissipation coupled with diminishing performance gains, was also the main cause for the switch from single-core to multi-core architectures and a slowdown in frequency increase. This book aims to document some of the most important architectural techniques that were invented, proposed, and applied to reduce both dynamic power and static power dissipation in processors and memory hierarchies.

Morgan & Claypool Publishers - Computer Architecture ...
There are two major approaches to processor architecture: Complex Instruction Set Computer (CISC, pronounced “Sisk”) processors and Reduced Instruction Set Computer (RISC) processors. Classic CISC processors are the Intel x86, Motorola 68xxx, and National Semiconductor 32xxx processors, and, to a lesser degree, the Intel Pentium. Common RISC architectures are the Freescale/IBM PowerPC, the MIPS architecture, Sun’s SPARC, the ARM, the Atmel AVR, and the Microchip PIC.

1. An Introduction to Computer Architecture - Designing ...
Techniques for improving programmability such as cache coherence increase cost and power consumption. Therefore, in designing the memory subsystem of a computer system, extensive knowledge and expertise, as well as careful attention to the target market and practical design constraints, is crucial to success.

Computer Architecture and Systems • Electrical and ...
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Computer Architecture Techniques for Power-Efficiency ...
This paper examines the interaction between thermal management techniques and power boosting in a state-of-the-art heterogeneous processor consisting of a set of CPU and GPU cores. We show that for...

Cooperative boosting: needy versus greedy power management ...
In this paper, we illustrate the application of two static techniques to reduce the activities of the branch predictor in a processor leading to its significant power reduction. We introduce the use of a static branch target buffer (BTB) that achieves the similar performance to the traditional branch target buffer but eliminates most of the state updates thus reducing the power consumption of the BTB significantly.